

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

Express Mail No.: EK 742 525 445US
Date of Deposit: December 28, 2001

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Address" Service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner of Patents, Washington, D.C. 20231.

December 28, 2001
Date of Signature


Stephen A. Gratton
Attorney for Applicants

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

**METHOD FOR FABRICATING
SEMICONDUCTOR COMPONENTS AND
INTERCONNECTS WITH CONTACTS ON
OPPOSING SIDES**

INVENTORS

**WARREN M. FARNWORTH
ALAN G. WOOD
DAVID R. HEMBREE**

ATTORNEY'S DOCKET NO. 97-1363.3

204070 "SSEEDOT"

Cross Reference To Related Applications

This application is a continuation-in-part of application serial no. 09/961,646 filed September 24, 2001, which is a division of application serial no. 09/385,606, filed on August 30, 1999, Patent No. 6,294,387, which is a division of application serial no. 08/993,965, filed on December 18, 1997, Patent No. 6,107,109.

Field of the Invention

This invention relates generally to semiconductor manufacture, and specifically to a method for fabricating semiconductor components and interconnects with contacts on opposing sides.

Background of the Invention

Semiconductor components include external contacts that allow electrical connections to be made from the outside to the integrated circuits contained on the components. A semiconductor die, for example, includes patterns of bond pads formed on the face of the die. Semiconductor packages, such as chip scale packages, also include external contacts. One type of semiconductor package includes solder balls arranged in a dense array, such as a ball grid array (BGA), or fine ball grid array (FBGA).

Typically, a component includes only one set of external contacts on either the face side (circuit side) or the back side of the component. However, it is sometimes necessary for a component to have external contacts on both sides. For example, for stacking a semiconductor package to another identical package, external contacts can be formed on the face of the package and on the back side as well. U.S. Patent No. 6,271,056 to Farnworth et al. discloses this type of stackable package.

Interconnects configured to make electrical connections with semiconductor components also include external contacts.

A wafer probe card is one type of interconnect adapted to make electrical connections between external contacts on a wafer under test, and test circuitry associated with a wafer handler. Another type of interconnect is adapted to electrically engage unpackaged dice, or chip scale packages, packaged within a test carrier. U.S. Patent No. 5,541,525 to Wood et al. discloses this type of interconnect and test carrier.

In each of these examples, the interconnect includes external contacts for electrically engaging the external contacts on the semiconductor component. With a conventional needle probe card the external contacts comprise probe needles. With an interconnect used with a test carrier as described above, the interconnect contacts can comprise projections formed on a silicon substrate and covered with a conductive layer.

As with semiconductor components, the external contacts for an interconnect are often formed on both sides of the interconnect. For example, a probe card can include contacts on its face for electrically engaging the component, and contacts on its back side for electrically engaging spring loaded pins (e.g., "POGO PINS") in electrical communication with test circuitry. U.S. Patent No. 6,060,891 to Hembree et al. discloses this type of interconnect.

The present invention is directed to a method for fabricating semiconductor components and interconnects with contacts on opposing sides.

Summary of the Invention

In accordance with the present invention, a method for fabricating semiconductor components and interconnects is provided. Also provided are improved components and interconnects fabricated using the method, and improved electronic assemblies and test systems incorporating the components and the interconnects.

Initially a substrate having a face side, an opposing back side and a plurality of substrate contacts on the face side. For fabricating semiconductor components, such as packages, the substrate can comprise a semiconductor die containing integrated circuits. The substrate contacts can comprise bond pads in electrical communication with the integrated circuits. For fabricating interconnects the substrate can comprise a semiconductor, a ceramic or a plastic. In addition, the substrate contacts can be dummies or omitted entirely.

The method also includes the step of forming vias through the substrate using a laser beam directed through the substrate contacts. The method also includes the steps of forming conductive members in the vias, and then forming external contacts on the face side and the back side of the substrate in electrical communication with the conductive members. The external contacts can also include a non-oxidizing layer which facilitates making permanent or temporary electrical connections with the external contacts. The external contacts on the face side and the back side can have matching patterns that allows identical components to be stacked to one another. Alternately the external contacts on the face side and the back side can be offset or redistributed with respect to one another.

A semiconductor component, such as a die, a package or a wafer, fabricated using the method, includes the substrate and the external contacts on the face side and the back side. The external contacts on the face side can be bonded to external contacts on the back side of an identical component to make a stacked assembly. An interconnect fabricated using the method includes the external contacts on the face side which can be configured to electrically engage a semiconductor component. The interconnect also includes external contacts on the back side which can be configured to

electrically engage electrical connectors associated with test circuitry.

5 In an alternate embodiment of the method, the vias are initially formed as counter bores, and the conductive members are formed in the vias. The substrate is then thinned from the back side using a thinning process, such as chemical mechanical planarization (CMP) or etching, to expose the conductive members.

10 An electronic assembly includes multiple stacked components fabricated using the method. Another electronic assembly includes an interconnect fabricated using the method having semiconductor components attached to opposing sides. A test system for testing singulated components, such as dice and packages, includes a die level interconnect mounted to a test carrier configured to temporarily package the components. A test system for testing wafers, or other substrates containing multiple components, includes a wafer level interconnect mounted to a test apparatus such as a wafer prober.

Brief Description of the Drawings

20 Figures 1A-1G are schematic cross sectional views illustrating a method for fabricating semiconductor components and interconnects on a substrate in accordance with the invention;

25 Figure 2A is a top view taken along line 2A-2A of Figure 1B illustrating a substrate contact on the substrate;

30 Figure 2B is a top view taken along line 2B-2B of Figure 1D illustrating the substrate contact following an etching step but prior to a laser drilling step;

Figure 2C is a top view taken along line 2C-2C of Figure 1D illustrating the substrate contact following the laser drilling step;

Figures 3A-3F are schematic cross sectional views illustrating an alternate embodiment method for fabricating semiconductor components and interconnects;

Figure 4A is a schematic side elevation view illustrating an electronic assembly fabricated using stackable components fabricated using the method;

Figure 4B is a plan view taken along line 4B-4B of Figure 4A;

Figure 5A is a schematic cross sectional view illustrating an electronic assembly that includes an interconnect fabricated using the method;

Figure 5B is a cross sectional view taken along section line 5B-5B of Figure 5A;

Figure 6 is a schematic cross sectional view illustrating a test system that includes an interconnect fabricated using the method;

Figures 7A and 7B are schematic perspective views illustrating a test system that includes a die level interconnect fabricated using the method;

Figure 7C is an enlarged cross sectional view taken along section line 7C-7C of Figure 7B;

Figure 8 is a schematic view illustrating a test system that includes a wafer level interconnect fabricated using the method;

Figure 9 is a schematic side elevation view illustrating an electronic assembly fabricated using stackable components fabricated using the method;

Figure 10A is a schematic side elevation view illustrating an electronic assembly fabricated using stackable components fabricated using the method; and

Figure 10B is a plan view taken along line 10B-10B of Figure 10A.

Detailed Description of the Preferred Embodiments

As used herein, the term "semiconductor component" means an electronic component that includes a semiconductor die.

5 Exemplary semiconductor components include bare semiconductor dice, chip scale packages, ceramic or plastic semiconductor packages, BGA devices, semiconductor wafers, and panels and leadframes containing multiple dice or chip scale packages.

10 An "interconnect" means an electronic component configured to make electrical connections with a semiconductor component. A die level interconnect can be configured to electrically engage singulated components such as a die or a package. A wafer level interconnect can be configured to electrically engage a substrate, such as a
15 wafer, a panel, or a leadframe, containing multiple components.

Referring to Figures 1A-1G, a method for fabricating semiconductor components and interconnects in accordance with the invention is illustrated. Initially as shown in Figure
20 1A, a substrate 10 is provided. Preferably, the substrate 10 comprises a wafer of material on which multiple components or interconnects will be fabricated using semiconductor circuit fabrication techniques, and then singulated by cutting the wafer.

25 If the semiconductor component being fabricated is a package, such as a chip scale package, the substrate 10 can comprise a semiconductor die containing a plurality of integrated circuits. The die in turn can be contained on a wafer which includes a plurality of dice which are then
30 singulated into individual packages. Depending on the application, the die can be configured as a memory device, as a vertical cavity surface emitting laser device (VCSEL), or in any other conventional configuration.

If the semiconductor component being fabricated is an
35 interconnect, the substrate can comprise a semiconductor

material such as monocrystalline silicon, germanium, silicon-on-glass, or silicon-on-sapphire. These materials have a TCE (thermal coefficient of expansion) that matches, or is close to, the TCE of the mating semiconductor component which the interconnect engages. Alternately, the substrate 10 can comprise a ceramic material, such as mullite, or a plastic material, such as a glass filled resin (e.g., FR-4).

The substrate 10 includes a face side 14 ("first side" in the claims) and an opposing back side 16 ("second side" in the claims). The face side 14 and the back side 16 are the major planar surfaces of the substrate 10, and are generally parallel to one another. A representative thickness of the substrate 10 can be from about 12 mils to 38 mils. A peripheral size and shape of the substrate 10 can be selected as required. For example, semiconductor dice have generally rectangular or square peripheral shapes.

As shown in Figure 1A, the substrate 10 can include substrate contacts 18, and a front side insulating layer 20. The substrate contacts 18 are formed of a highly conductive metal such as aluminum, titanium, nickel, iridium, copper, gold, tungsten, silver, platinum, palladium, tantalum, molybdenum or alloys of these metals. If the substrate 10 is a semiconductor die, the substrate contacts 18 can be the device bond pads, or alternately redistribution layer pads, in electrical communication with the integrated circuits contained on the die.

If an interconnect is being fabricated, the substrate contacts 18 can be dummy contacts, or can be omitted entirely. As shown in Figure 2A, the substrate contacts 18 have a generally square peripheral shape. However, other shapes such as rectangular, circular or oval can also be employed. A size of the substrate contacts 18 can also be selected as required (e.g., 10-100µm on a side).

The front side insulating layer 20 can comprise an electrically insulating material deposited to a desired

thickness using a suitable deposition process (e.g., CVD, sputtering, spin-on). Exemplary materials include glass materials such as BPSG, oxide materials, such as SiO₂, or polymer materials, such as polyimide. If the substrate 10 is a die, the front side insulating layer 20 can be the outer passivation layer for the die. A thickness for the front side insulating layer 20 will be dependent on the material. For example oxide materials can be deposited to thicknesses of 500Å or less, and polymer materials can be deposited to thicknesses of several mils or more.

As shown in Figure 1B, a back side insulating layer 22 is blanket deposited on the back side 16 of the substrate 10. The purpose of the back side insulating layer 22 is to provide electrical insulation for the back side 16. The back side insulating layer 22 can be formed of the same materials as previously described for the front side insulating layer 20 using a suitable deposition process (e.g., CVD, sputtering, spin-on).

As shown in Figure 1C, a front side protective mask 24 is formed on the front side insulating layer 20, and a back side protective mask 26 is formed on the back side insulating layer 22. Preferably the protective masks 24, 26 comprise a photoimageable material, such as a photoresist, or a photoimageable polymer, such as polyimide. The protective masks 24, 26 can be deposited using a suitable deposition process such as spin-on and then soft baked to drive out solvents. Depending on the material, a representative thickness for the protective masks 24, 26 can be from 10,000Å to 50µm. Following the softbake, the front side protective mask 24 is aligned with a mask and exposed using UV light.

As shown in Figure 1D, the front side protective mask 24 is developed to form openings 28 aligned with the substrate contacts 18. The substrate contacts 18 are then etched such that the openings 28 also extend through the substrate contacts 18 to the substrate 10. Depending on the material

for the substrate contacts 18 a wet etchant can be used to etch the substrate contacts 18. For example, for substrate contacts 18 made of aluminum, one suitable wet etchant is H_3PO_4 .

5 Figure 2B illustrates the mask 24 and the substrate contacts 18 following the etching step but prior to a laser drilling step. As shown in Figure 2B, the openings 28 in the mask 24 and in the substrate contacts 18 are generally circular, and are smaller in diameter than the width of the
10 substrate contacts 18. The substrate contacts 18 thus have metal around their peripheries but no metal in the center. In the illustrative embodiment the openings 28 have a diameter that is about half the width of the substrate contacts 18. In addition, the openings 28 surround a portion
15 of the substrate 10, such that the substrate contacts 18 and the openings 28 form targets, or bullseyes, for a subsequent laser drilling step in which a laser beam 33 (Figure 1D) is directed at the openings 28 and through the substrate 10. The laser beam 33 (Figure 1D) initially pierces the substrate
20 10 on the portions of the substrate 10 surrounded by the openings 28.

As shown in Figure 1D, the laser drilling step forms lasered openings 29 through the substrate 10, through the back side insulating layer 22 and through the back side
25 protective mask 26. Figure 2C illustrates the mask 24 and the substrate contacts 18 following the laser drilling step.

As shown in Figure 2C, the lasered openings 29 do not touch the metal of the substrate contacts 18, as they are located in the middle of the openings 28 in the substrate
30 contacts 18. In the illustrative embodiment, the lasered openings 29 have diameters that are about half the diameters of the openings 28. The laser beam 33 (Figure 1D) thus initially contacts and pierces the substrate 10 without having to contact and pierce the metal that forms the
35 substrate contacts 18. This eliminates shorting between the

completed external contacts 38 (Figure 1G) and the substrate 10 because any conducting or semiconducting material redeposited by penetration of the laser beam 33 will not contact the external contacts 38.

5 Following the laser drilling step, a cleaning step can be performed in which the lasered openings 29 are cleaned using a suitable wet or dry etchant. One suitable wet etchant for cleaning the lasered openings 29 with the substrate 10 comprising silicon is
10 tetramethylammoniumhydroxide (TMAH).

As shown in Figure 1E, the cleaning step forms vias 30 which extend through the substrate 10, through the back side insulating layer 22, and through the back side protective mask 26. In the illustrative embodiment the vias have
15 diameters that are about twice the inside diameters of the lasered openings 29, and about equal to the inside diameters of the openings 28. By way of example, the diameters of the vias 30 can be from 10 μ m to 2 mils or greater.

A suitable laser system for performing the laser
20 drilling step is manufactured by Electro Scientific, Inc., of Portland, Oregon and is designated a Model No. 2700. A representative laser fluence for forming the vias 30 through a silicon substrate having a thickness of about 28 mils, is from 2 to 10 watts/per opening at a pulse duration of 20-25
25 ns, and at a repetition rate of up to several thousand per second. The wavelength of the laser beam can be a standard UV wavelength (e.g., 455 nm).

As shown in Figure 1E, the vias 30 are preferably generally perpendicular to the face side 14, and to the back
30 side 16 of the substrate 10. In addition, the vias 30 are located along a longitudinal axis 31 which preferably extends through the centers of the openings 28 in the front side protective mask 24 and the substrate contacts 18. The openings 28 and the substrate contacts 18 thus provide
35 targets for aligning the laser beam. In addition, the

openings 28 help to compensate for misalignment of the laser beam because the openings 28 will subsequently determine the peripheral shape of the external contacts 38 (Figure 1G). Further, during the laser drilling step the protective masks 5 24, 26 protect the face side 14 and the back side 16 of the substrate 10.

As also shown in Figure 1E, following formation of the vias 30, insulating layers 32 can be formed on the inside surfaces of the vias 30. The insulating layers 32 10 electrically insulate the vias 30 from the rest of the substrate 10, and are required if the substrate 10 comprises a semiconductor material. The insulating layers 32 can be a grown or deposited material.

With the substrate 10 comprising silicon, the insulating layers 32 can be an oxide, such as SiO_2 , formed by a growth process by exposure of the substrate 10 to an O_2 atmosphere at an elevated temperature (e.g., 950°C). In this case the insulating layers 32 do not completely close the vias 30, but form only on the sidewalls of the vias 30. Alternately, the 20 insulating layers 32 can comprise a deposited electrically insulating material, such as an oxide or a nitride, deposited using a deposition process such as CVD.

The insulating layers 32 can also comprise a polymer material deposited using a suitable deposition process such as screen printing. In this case, if the insulating material completely fills the vias 30, a subsequent laser drilling step, substantially as previously described, may be required to re-open the vias 30. If the substrate 10 comprises an electrically insulating material, such as ceramic, or a glass 30 filled resin, such as FR-4, the insulating layers 32 are not required.

Following formation of the insulating layers 32, conductive members 34 (Figure 1G) can be formed within the vias 30. The conductive members 34 can be plugs that 35 completely fill the vias 30, or alternately, can be layers

that cover just the inside surfaces or sidewalls of the vias 30. The conductive members 34 can comprise a highly conductive metal, such as aluminum, titanium, nickel, iridium, copper, gold, tungsten, silver, platinum, palladium, tantalum, molybdenum or alloys of these metals. The above metals can be deposited within the openings 28 using a deposition process, such as electroless deposition, CVD, or electrolytic deposition. Alternately a solder metal can be screen printed in the vias 30 and drawn into the vias 30 with capillary action. A solder metal can also be drawn into the vias 30 using a vacuum system and a hot solder wave.

Rather than being a metal, the conductive members 34 can comprise a conductive polymer, such as a metal filled silicone, or an isotropic epoxy. Suitable conductive polymers are sold by A.I. Technology, Trenton, NJ; Sheldahl, Northfield, MN.; and 3M, St. Paul, MN. A conductive polymer can be deposited within the vias 30, as a viscous material, and then cured as required. A suitable deposition process, such as screen printing, or stenciling, can be used to deposit the conductive polymer into the vias 30.

In the embodiment illustrated in Figures 1A-1G, the conductive members 34 are formed by an electroless deposition process. To perform the electroless deposition process, a seeding step is performed in which the substrate 10, with the protective masks 24, 26 thereon, is dipped in a seed solution. Seed solutions for electroless deposition of various metals are known to those skilled in the art. For example, for depositing copper conductive members 34 the seed solution can comprise a copper sulfate solution available from Shipley. The seed solution adheres to all exposed surfaces including on the protective masks 24, 26 and in the openings 28.

As shown in Figure 1F, following the seeding step, a stripping step is performed in which the protective masks 24, 26 are stripped. Depending on the material for the masks 24,

26, the stripping step can be performed using a suitable stripper or solvent. For example, acetone and methylethylketone can be used for a positive resist, and a solution of H_2SO_4 and H_2O_2 can be used for a negative resist.

5 However, the stripper must be selected to not attack the seed solution which adheres to the sidewalls of the vias 30.

10 Next, as shown in Figure 1G, an electroless deposition step is performed in which a metal is electrolessly deposited into the vias 30 to form the conductive members 34. The electroless deposition step can be performed by dipping the substrate 10 in a suitable electroless deposition solution. For example, for depositing copper conductive members 34, the electroless deposition solution can comprise a nickel hypophosphate solution available from Shipley or Packaging Technology of Nauen, Germany.

15 As shown in Figure 1G, the electroless deposition step forms the conductive members 34 with generally concave terminal portions 36 (dish shaped buttons) on the insulating layers 20, 22. As will be further explained, the concave terminal portions 36 facilitate making electrical connections with bumped contacts, such as solder balls or bumps. The conductive members 34 are also in electrical communication with the substrate contacts 18. In addition, the conductive members 34 at least partially fill the vias 30, and physically contact the substrate contacts 18.

20 As also shown in Figure 1G, following formation of the conductive members 34, non-oxidizing metal layers 42 are formed on the concave terminal portions 36 of the conductive members 34. The non-oxidizing metal layers 42 can be formed using a suitable deposition process such as electroless deposition or CVD. With electroless deposition, a mask is not required, as the substrate 10 is dipped into a suitable solution and deposition onto the terminal portions 36 occurs as previously described. With CVD, a mask (not shown) can be formed on the insulating layers 20, 22, having openings

aligned with the terminal portions 36 of the conductive members 34. The non-oxidizing metal can then be deposited through the openings to a desired thickness.

Suitable metals for the non-oxidizing metal layers 42 include gold, platinum, and palladium. A representative thickness for the non-oxidizing metal layers 42 can be from 600Å to 3000Å or more. In addition, the non-oxidizing metal layers 42 have a concave shape substantially similar to that of the concave terminal portions 36. Following the depositing of the non-oxidizing metal layers 42 the substrate 10 can be singulated into individual components or interconnects if required using a suitable process such as sawing, shearing, punching or etching.

As shown in Figure 1G, the face side insulating layer 20 on the face side 14 of the substrate 10 includes face side external contacts 38 ("first external contacts" in the claims). The back side insulating layer 22 on the back side 16 of the substrate 10 includes back side external contacts 40 ("second external contacts" in the claims).

The size and spacing of the face side external contacts 38 matches the size and the spacing of the back side external contacts 40, such that each face side external contact 38 has a mating back side external contact 40 located along a common longitudinal axis 31 (Figure 1E). Stated differently, the face side external contacts 38 and the back side external contacts 40 have matching patterns such as a dense grid array. As will be further explained, alternately the back side external contacts 40 can be "offset" or "redistributed" with respect to the face side external contacts 38.

The conductive members 34 establish electrical communication between the mating external contacts 38, 40 on the opposing sides of the substrate 10. In addition, the conductive members 34 establish electrical communication between mating external contacts 38, 40 and the substrate contacts 18. If the substrate 10 includes integrated

circuits in electrical communication with the substrate contacts 18, the external contacts 38, 40 are also in electrical communication with the integrated circuits.

Referring to Figures 3A-3F, an alternate embodiment method for fabricating semiconductor components and interconnects is illustrated. Initially, as shown in Figure 3A, a substrate 10A is provided having a front side 14A, a back side 16A, substrate contacts 18A and a front side insulating layer 20A as previously described.

As shown in Figure 3B, a front side protective mask 24A is formed on the front side 14A of the substrate 10A. The mask 24A is then used to etch openings 28A in the substrate contacts 18A as previously described. In addition, lasered openings 29A are formed in the substrate 10A by directing a laser beam 33A through the substrate 10A as previously described. However, in this case the laser drilling step is performed such that the laser openings 29A are counter bores that do not extend completely through the substrate 10A. For forming the laser openings 29A, parameters of the laser system, such as beam power, power distribution, pulse length and pulse duration of the laser beam 33, can be adjusted such that the substrate is not pierced.

Next, as shown in Figure 3C, a cleaning step is performed in which the lasered openings 29A are cleaned and enlarged as previously described to form vias 30A. Again the vias 30A are counter bores that do not extend completely through the substrate 10A. As also shown in Figure 3C, insulating layers 32A are formed in the vias 30A as previously described.

Next, as shown in Figure 3D, conductive members 34A are formed in the vias 30A. The conductive members 34A can comprise a metal or a conductive polymer deposited as previously described using a deposition process such as CVD or screen printing. However, in this case the mask 24A is retained, and the conductive members 34A are also formed in

the openings 28A and have surfaces generally planar to a surface of the mask 24A.

Next, as shown in Figure 3E, the mask 24A is stripped as previously described. In addition, a thinning step is performed in which the substrate 10A is thinned from the back side 16A to form a thinned substrate 10A-T. In addition, the thinning step is controlled to planarize and expose the conductive members 34A on a thinned back side 16A-T of the thinned substrate 10A-T. One process for performing the thinning step is chemical mechanical planarization (CMP). One suitable CMP apparatus for performing the thinning step is a Model 372 manufactured by Westech. The thinning step can also be performed by etching the back side 16A of the substrate 10A using a suitable etchant.

Next, as shown in Figure 3F, non-oxidizing layers 42A are formed on the conductive members 34A, as previously described. However, unless the substrate 10 comprises an electrically insulating material such as ceramic or plastic, the non-oxidizing layers 42A on the thinned back side 16A-T must only contact the conductive members 34A and insulating layers 32A. The completed front side external contacts 38A and back side external contacts 40A function substantially as previously described.

Referring to Figures 4A and 4B, an electronic assembly 52 constructed using stackable components 54-1, 54-2 fabricated in accordance with the method of the invention are illustrated. In this embodiment, the stackable components 54-1, 54-2 are in the form of singulated packages having a chip scale configuration. However, it is to be understood that the stackable components 54-1, 54-2 can also comprise stackable semiconductor dice, stackable semiconductor wafers or stackable panels. In addition, although only two components 54-1, 54-2 form the assembly 52, it is to be understood that any number of stackable components can be utilized.

1003556 040402
204040 5555001

5 In addition to the stackable components 54-1, 54-2, the electronic assembly 52 includes a supporting substrate 56, such as a printed circuit board or multi chip module substrate, having a plurality of metal electrodes 58. The stackable components 54-1, 54-2 are stacked to one another with the back side external contacts 40 on the lowermost component 54-1 bonded to the electrodes 58 on the supporting substrate 56. In addition, the front side external contacts 38 on the lowermost component 54-1 are bonded to the back side external contacts 40 on the uppermost component 54-2. The external contacts 38, 40 can be bonded to one another by heating and reflowing the metal of the external contacts 38, 40. Alternately, solder and a solder reflow process can be used to bond the external contacts 38, 40 to one another. In either case the non-oxidizing layers 42 (Figure 1G) on the external contacts 38, 40 facilitate the bonding process, and prevent the formation or resistance increasing oxide layers.

20 Referring to Figures 5A and 5B, an electronic assembly 60 constructed using an interconnect 66 fabricated in accordance with the invention is illustrated. In this embodiment, the electronic assembly 60 is in the form of a multi chip module. The interconnect 66 includes front side external contacts 38 and back side external contacts 40 as previously described. In addition, the interconnect 66 includes conductors 68 in electrical communication with the contacts 38, 40 and edge contacts 70 in electrical communication with the conductors 68.

30 The electronic assembly 60 also includes a semiconductor package 62-1 having bumped contacts 64, such as solder bumps or balls, bonded to the front side external contacts 38 on the interconnect 66. In addition, the electronic assembly 60 includes a semiconductor package 62-2 having bumped contacts 64 bonded to the back side external contacts 40 on the interconnect 66. Again, a reflow process or a soldering

process can be used to bond the bumped contacts 64 to the external contacts 38, 40.

Referring to Figure 6, a test assembly 72 constructed using an interconnect 74 fabricated in accordance with the invention is illustrated. The test assembly 72 includes test circuitry 84 configured to generate and apply test signals to a device under test 76. By way of example, the device under test 76 can comprise a die, a package, a wafer or a panel having bumped contacts 78. The test circuitry 84 is in electrical communication with the back side external contacts 40 on the interconnect 74. The front side external contacts 38 establish temporary electrical connections with the device contacts 78.

Referring to Figures 7A-7C, a die level test system 80 constructed with an interconnect 86 fabricated in accordance with the invention is illustrated. The test system 80 is configured to temporarily package and test multiple semiconductor components 88 such as dice, packages, or BGA devices having bumped contacts 90.

The test system 80 includes the interconnect 86 which is configured to electrically engage the bumped contacts 90 on the components 88. The test system 80 also includes an alignment member 92 configured to align the components 88 on the interconnect 86, and a force applying mechanism 94 with elastomeric members 98 configured to bias the components 88 and the interconnect 86 together.

The interconnect 86 includes the front side external contacts 38 formed as previously described, and configured to make temporary electrical connections with the bumped contacts 90 on the components 88. In addition, the interconnect 86 includes the back side external contacts 40 formed as previously described but with terminal contacts 96, such as solder balls attached thereto. The terminal contacts 96 are configured for mating electrical engagement with a test apparatus 82, such as a test socket or burn-in board in

electrical communication with test circuitry 84. The test circuitry 84 is configured to apply test signals to the integrated circuits contained on the components 88 and to analyze the resultant signals.

5 As shown in Figure 7B, the force applying mechanism 94 attaches to the alignment member 92 and the interconnect 86, and biases the components 88 and the interconnect 86 together. As shown in Figure 7C, the alignment member 92 includes tapered alignment openings 100 configured to align
10 the components 88 on the interconnect 86.

Referring to Figure 8, a wafer level test system 102 suitable for testing a wafer sized semiconductor component 104 with bumped contacts 106 is illustrated. By way of example, the semiconductor component 104 can comprise a
15 semiconductor wafer containing bare dice, a wafer or panel containing chip scale packages, a printed circuit board containing semiconductor dice, or an electronic assembly, such as a field emission display containing semiconductor dice.

20 The wafer level test system 102 includes an interconnect 108 constructed as previously described, and mounted to a testing apparatus 110. The testing apparatus 110 includes, or is in electrical communication with test circuitry 84. The testing apparatus 110 also includes a wafer chuck 116
25 configured to support and move the component 104 in x, y and z directions as required. The testing apparatus 110 can comprise a conventional wafer probe handler, or probe tester, modified for use with the interconnect 108. Wafer probe handlers and associated test equipment are commercially
30 available from Electroglass, Advantest, Teradyne, Megatest, Hewlett-Packard and others. In this system 102, the interconnect 108 takes the place of a conventional probe card.

35 The interconnect 108 includes the previously described front side external contacts 38 configured to establish

temporary electrical connections with the bumped contacts 106 on the component 108. In addition, the interconnect 108 includes the previously described back side external contacts 40 configured to electrically engage spring loaded electrical connectors 114 (e.g., "POGO PINS" manufactured by Pogo Instruments, Inc., Kansas City, KS) in electrical communication with the testing circuitry 112.

Referring to Figure 9, an electronic assembly 118 constructed using stackable components 54B-1, 54B-2, 54B-3, 54B-4 fabricated in accordance with the method of the invention are illustrated. In this embodiment, the stackable components 54B-1, 54B-2, 54B-3, 54B-4 are in the form of singulated packages having a chip scale configuration substantially similar to the previously described stackable component 54. However, as before stackable semiconductor dice, stackable semiconductor wafers or stackable panels can be employed. In addition, although four components 54B-1, 54B-2, 54B-3, 54B-4 form the assembly 118, it is to be understood that any number of stackable components can be utilized.

Each stackable component 54B-1, 54B-2, 54B-3, 54B-4 includes face side external contacts 38B and back side external contacts 40B having matching patterns. Each stackable component 54B-1, 54B-2, 54B-3, 54B-4 also includes conductive members 34B formed using a laser machining process as previously described. In addition, the back side external contacts 40B include bumped contacts 120 such as solder balls or bumps attached thereto using a suitable process such as ball bumping, bump deposition or reflow bonding. The bumped contacts 120 and face side external contacts 40B on adjacent components 54B-1, 54B-2, 54B-3, 54B-4 are bonded to one another using a suitable bonding process such as reflow bonding.

Referring to Figures 10A and 10B, an electronic assembly 122 constructed using stackable components 54C-1, 54C-2, 54C-

3, 54C-4 fabricated in accordance with the method of the invention are illustrated. In this embodiment, the stackable components 54C-1, 54C-2, 54C-3, 54C-4 are in the form of singulated packages having a chip scale configuration substantially similar to the previously described stackable component 54. However, as before stackable semiconductor dice, stackable semiconductor wafers or stackable panels can be employed.

Each stackable component 54C-1, 54C-2, 54C-3 includes face side external contacts 38C and back side external contacts 40C having matching patterns. Each stackable component 54C-1, 54C-2, 54C-3 also includes conductive members 34C formed using a laser machining process as previously described. In addition, the back side external contacts 40C include bumped contacts 124 such as solder balls or bumps attached thereto using a suitable process such as ball bumping, bump deposition or reflow bonding. The bumped contacts 122 and face side external contacts 40C on adjacent components 54C-1, 54C-2, 54C-3 are bonded to one another using a suitable bonding process such as reflow bonding.

Although stackable components 54C-1, 54C-2, 54C-3 have identical configurations, the stackable component 54C-4 has a different configuration. Specifically, the back side external contacts 40C for stackable component 54C-4 are "offset" or "redistributed" with respect to the face side external contacts 38C. As shown in Figure 10B, redistribution conductors 126 on the back side of the stackable component 54C-4 are in electrical communication with the conductive members 34C and with the back side external contacts 40C. This arrangement allows the back side external contacts 40C to have a different pattern than the face side external contacts 38C. For example, a pitch P1 of the back side external contacts 38C can be greater than a pitch P2 of the face side external contacts 38C. This arrangement can be used to facilitate bonding of the

stackable component 54C-4 and thus the assembly 122 to a supporting substrate, such as a printed circuit board.

Thus the invention provides a method for fabricating semiconductor components and interconnect for semiconductor
5 components. The invention also provides improved electronic assemblies and test systems constructed using components and interconnects fabricated in accordance with the invention.

Although the invention has been described with reference
to certain preferred embodiments, as will be apparent to
10 those skilled in the art, certain changes and modifications can be made without departing from the scope of the invention as defined by the following claims.

204070 010402